REMARKS

Applicant will address the Office Action according to the order in which issues were raised therein. Like sub-headings will be used for convenience.

As a preliminary matter, however, Applicants address the "after final" aspects of this amendment.

No amendments to the claims are sought. Only amendments to the drawings and the specification. Applicants had made a good faith effort to address all previous drawing objections and apparently overlooked two minor, and obvious, reference numbering errors. Entry of the requested drawing corrections will impose no burden on the Office and will simplify the issues on appeal should an allowance not be forthcoming. The amendments to the specification are all minor in nature. Fig. 5 and the specification are conformed by the amendment to pages 13-14. In the amendment to page 17, reference to one switch is conformed to a drawing correction (see below); at the same time, a grammatical correction is made. Entry of the amendments to the specification will also simplify the issues on appeal. No new matter is entered and no additional search or other burden is imposed. Therefore, Applicants request entry of these amendments.

Drawings

The Examiner has objected that the drawings do not include reference signs for the SC DAC 150. Reconsideration is requested. Lines 28 and 30 of page 11, identified by the Examiner, refer to Fig. 4. The reference numeral 150 appears in the upper right corner of Fig. 4. No change to the figure is required.

The Examiner has also objected that Figs. 5 and 13 contain a reference numeral 152 not mentioned in the description. With respect to Fig. 5, reconsideration is requested. In the drawings correction submitted February 20, 2003, Fig. 5 was revised by deleting reference numeral 152. With respect to Fig. 13, a proposed correction is submitted herewith, deleting reference numeral 152.

The drawing objections have thus been overcome.

In addition, an obvious error with respect to a reference numeral is corrected in Fig. 10. Switch S19 should have been switch S17, consistent with the labeling of that switch in other figures.

Claim rejections - 35 USC §112

Claims 1-52 have been rejected under 35 USC §112, first paragraph, as not being enabled by the specification. The Examiner then lists a number of points with respect to things he does not understand in the specification. However, he never relates them to the claimed subject matter. Accordingly, this rejection is improper in form and content. Applicant will attempt to address the issues raised by the Examiner and to clarify his understanding, but without a clear rejection explaining why a given claim is not enabled, Applicant does not know what portion of the specification the Examiner has looked to for support of a given claim element. Thus, the Office Action really does not afford Applicants a proper basis for understanding the rejection or for providing the Examiner with the kind of response he requires. All claims are, indeed, properly enabled by the specification.

Under Paragraph 5(a), the Examiner indicates that he does not understand how the switched capacitor, the sub DACs, elements QDAC1 to QDACN and the charge sharing network in Fig. 4 are interconnected with each other since the interconnecting relationship is not described in the specification as well as is shown in any drawings of the present invention. It may help to point out to the Examiner that the notations Q_{DAC1}... Q_{DACN} relate not to elements but to the charges (Q being the conventional symbol for charge) for each of the respective sub DACs. As stated on page 12, the DAC 150 comprises four switched capacitor DACs, sometimes referred to as sub-DACs. The text goes on to explain that a first one of the sub-DACs has a reference voltage connected to a first terminal of the switch, etc. On page 12, at lines 4-5, it is expressly stated that each of the sub-DACs shares charge via a charge sharing network with at least one other of the sub-DACs. The details as to how that charge sharing occur in a specific embodiment are specified at, for example, page 12, line 15-page 14, line 32. Other embodiments are discussed in connection with Figs. 8A-8D, commencing on page 16, at line 15, and elsewhere in connection with other figures. Accordingly, the interconnection and charge sharing of the sub-DACs is extensively described. Indeed, it is described in greater detail than is required for one skilled in the art to understand the invention and how it may be practiced.

In item 5(b), the Examiner expresses that it is not understood what the SC DAC 150, from page 11, lines 28 and 30, really is, because it is not shown in Fig. 4. As stated above, Fig. 4 clearly contains the reference numeral 150 which pertains to the entirety of Fig. 4. There is nothing here unclear or requiring clarification.

In item 5(c), the Examiner indicates that it is not understood what the number 152 in Figs. 5 and 13 really is. The point is taken. That reference number has been deleted from Fig. 13 and was already deleted with respect to Fig. 5.

The Action further indicates "it is not understood how the P1 signal can control switch S13... since P1+P2 signal is seen to be provided to switch S13 in Fig. 5." The Examiner's puzzlement is now, finally, understandable. The specification on pages 13 and 14 has been amended in a way that should resolve that puzzlement. The specification is more closely conformed to Fig. 5. The specification now makes clear that switch S13 is controlled by the P1+P2 signal, which is the logical – OR of the P1 and P2 signals.

In item 5(d), the Office Action asserts that the switching on/off operation of each of the switches in each of a long list of figures "is not understood since no P1+P2 and P1-P3 switching control signals in Fig. 6 or P1-P4 switching control signals in Fig. 9 are seen to be respectively associated with each of the corresponding switches and the switching on/off operation of each of these switches is also not described in the specification." Reconsideration is requested. In the previous drawing correction, which the Examiner has already accepted, a waveform for P1+P2, which is merely the logical-OR of the waveforms for P1 and P2, was added.

As to a supposed lack of association between the switching control signals and the corresponding switches, we direct the Examiner's attention first to Figs. 7A-7C. There, each of the switches S13-S17 is the same as the correspondingly labeled switch in Fig. 5, where the control signal for each switch is expressly shown using a notation next to the switch, such as P1, P2, etc. The control signal is not indicated again in Figs. 7A-7C as it would be redundant to do so and would merely obfuscate the point being made in connection with the explanation of Figs. 7A-7C. So the switching operation and control of all of the switches in Figs. 7A-7C is fully documented in the specification and the drawings.

With respect to Figs. 8A-8D, it is stated on page 16, lines 20-22, "the embodiment shown in FIGS. 8A-8D is the same as that shown in Fig. 5 and Figs. 7A-7C, except at switches S18-S24 replace switches S13-S17." So control of switches S18-S24 has been explicitly disclosed.

With respect to Fig. 10, a drawing correction is being made herewith with respect to the label on the output switch, which should have been S17, not S19.

With respect to Figs. 11A-11D, page 17 expressly states at lines 31-33 that "the embodiment shown in Figs. 11A-11D is the same as that shown in Fig. 5 and Figs. 7A-7C, except that switches S18-S27 replace switches S13-S17."

Applicant offers to go through each of the other figures identified by the Examiner, if necessary, to establish to his satisfaction that the specification amply establishes the association between the switches and the control signals. However, as already demonstrated, such association clearly has been disclosed. Any lack of understanding at this point is not due to any fault of the specification or the drawings.

In item 5(e), the Examiner indicates that "it is not understood how P1+bit1·P2, . . . control signals as shown in Fig. 31 and as described in lines 4-15, page 34 ... can control the switching ... operation of the corresponding switches ... since the waveforms of each of P1+bit1·P2 etc. control signals are not seen in any drawings of the present invention." The Examiner's concern is unjustified and the nature of what he does not understand is not at all clear. Applicants must presume that the Examiner understands their Boolean expressions. For example, P1+bit1·P2 means that the value of bit1 is logically "AND-ed" with the P2 signal value and the result of that AND operation is then "OR-ed" with the P1 signal. Any electrical engineering graduate would be able to draw the waveform that results from this logical operation, given waveforms for P1 and P2. Therefore, providing the Boolean expression is equivalent to providing the waveform. The Examiner is thus without justification for requiring that the waveforms be drawn expressly, assuming that is what he is asking for. If the Examiner is taking the position that the Boolean algebra is not understood, Applicants would be happy to supply excerpts from any number of textbooks, but it is not seen at this time that the same should be required. Reconsideration is therefor requested.

In item 5(f) the Office Action states "it is not understood what all the P1-P3 signals in Fig. 32 are intended to use for applying into which corresponding switches in which respective embodiments of the present invention." Applicants take this unclear statement to mean that the Examiner does not believe that an electrical engineer will know how to build the logic circuits that will generate from the waveforms of Fig. 32 the control signals for the switches in Fig. 31. Such a position is completely untenable. These days, high school students, let alone graduate engineers, know how to combine basic logic gates in order to perform common Boolean logic. Is the Examiner requiring that the actual AND gates and OR gates (or, equivalently, NAND gates and NOR gates) be drawn to create the control signals in Fig. 31 from the waveforms of Fig. 32, and treating the disclosure as non-enabling without them? One hopes not. It would be a trivial exercise for any competent DAC engineer, no matter how inexperienced, to put together the gates/circuits to create the control signals once presented with the Boolean expressions to be implemented. So it is actually more instructive and more intelligible to provide the Boolean expressions than to draw the gates.

In view of the foregoing points, this rejection should now be withdrawn.

Claim rejections - 35 USC §103

Claims 1-4 and 13-51 have been rejected under 35 USC §103(a) as unpatentable over Fling, Mehta et al, and Lee et al. This is a repetition of a prior rejection to which Applicant has provided a full response in its February 13, 2003 amendment, which the Examiner addresses in his comments. However, the Examiner either misses an essential limitation of claim 1 or he mischaracterizes or misunderstands Fling '832 (the Office Action incorrectly uses the '831 number).

Claim 1 specifically requires that "the second analog signal also being indicative of ***said*** sum of values of ***said*** bits in the multi-bit digital signal." That is, the two analog signals which are output by the DAC are both indicative of the same sum of values of the **same** bits in the multi-bit digital signal. Referring to Fig. 1 of Fling, by contrast, it will be seen that there is a multiplexer (mux) which feeds to DACs 16 and 18 *alternating* portions of the samples on bus 13. As stated in column 2, lines 37-39, "Preconditioned samples on bus 13 are *alternately* applied via multiplexor 14 to DAC's 16 and 18." (Emphasis added.) Further it is stated in column 2, lines 59-60: "It will be understood that the operating phase of DAC 16 is *offset* from that of DAC 18." (Emphasis added.)

Manifestly, there is nothing that the secondary references can do or teach to change this basic aspect of the way Fling works. DACs 16 and 18 operate in ping-pong fashion. Consequently, there is absolutely no way that the outputs of those two DACs can both be indicative of a sum of values of the ***same bits*** in the multi-bit digital signal from bus 13. *They do not process the same bits* so they cannot output a signal derived from or indicative of any properties of the same bits. This is not an issue on which reasonable people can differ. It is plain black and white.

Nothing in either secondary reference teaches a change to Fling to get both DACs, contrary to the express teaching of Fling, to operate on the same input bits.

Moreover, as previously explained, Fling discloses only a DAC system having inside it **two DACs** (elements 16 and 18), **each of which outputs a *single* analog signal** (col. 2, lines 49-

58). In contrast, claim 1 recites a system having a **single** DAC that receives a multi-bit digital **and outputs at least *two* analog signals** (i.e., one DAC, but two output signals).

The secondary and tertiary references cannot completely alter the basic architecture of Fling in such a way as to eliminate its ping-pong operation on the input bits or to provide two analog signals from either of its DACs.

Consequently, the proposed combination simply does not achieve the claimed invention! In other words, the obviousness rejection is completely unsupportable and must be withdrawn.

Claim rejections - 35 USC §102

Claims 5-12 and 52 have been rejected as anticipated by Myers '724. However, Applicants' claims distinguish over Myers. Accordingly, reconsideration is requested.

1. Discussion of Myers

Myers is directed to an interpolating digital to analog conversion system that reduces the spurious energy content of the output signal in an effort to reduce the order of monolithically integrated reconstruction filters (Abstract; col. 1, lines 26-40). Myers teaches having a first conversion stage 22 which converts the least significant n bits of an N-bit signal and a second conversion stage 30 for combining the remainder of the N bits with the output of the first conversion stage 22 to provide an amplitude value output in line 28 (col. 2, lines 58-64). An interpolation stage 30 interpolates the amplitude value output to provide an interpolated amplitude output at node 32 at an interpolation output rate which is a multiple of the input rate of the N-bit digital signal (col. 2, lines 65-67).

2. Applicants' Claims Distinguish Over Myers

Claim 5 recites a system comprising: a DAC that receives a sequence of digital input signals at an input data rate and outputs a sequence of analog signals to a signal conditioning stage at an output data rate, each of the analog signals being indicative of an associated one of the digital input signals, the magnitude of the output data rate being different than the magnitude

of the input data rate, wherein more than one of the analog signals is generated during a single digital to analog conversion cycle of the DAC.

Myers does not disclose or suggest the system of claim 5. In particular, nowhere does Myers disclose or suggest a system in which **more than one** of the analog signals is generated during a single digital to analog conversion cycle of the DAC.

The Office Action states in its rejection that Myers discloses providing a sequence of output analog signals at an interpolation output data rate which is a multiple of the input data rate during a sampling time period, *and equates the sampling time period to a conversion cycle.* **However, contrary to this statement, nowhere does Myers suggest a system in which *more than one* of the analog signals is generated during a single digital to analog conversion cycle of the DAC**. Equating sampling time to a conversion cycle is improper and incorrect.

Myers discloses that each of the conversion stages makes use of a switched capacitor array such as that shown in Fig. 4 for the digital to analog conversion (col. 3, lines 4-24 and 30-36). As discussed in Myers and shown in Figs. 3 and 4, each of the capacitor arrays 40 and 50 and the overall DAC system of Fig. 3 have a single output. In addition, **the discussion of the operation of the capacitor array 40 shown in Fig. 4 makes it clear that only one output is provided by the capacitor array at output node 42, and that its output is provided at the sampling rate, as each of switches 44 are clocked at the sampling frequency (col. 3, lines 15-17).** Thus, not only is it not disclosed or suggested to generate more than one of the analog signals during a single digital to analog conversion cycle of the DAC, but also it is ***impossible*** for the system of Myers to do so!!!

The Examiner's logic failed when he equated sampling time to conversion cycle and when he failed to address how the output of the capacitor array is generated.

For at least the foregoing reasons, claim 5 patentably distinguishes over Myers. Accordingly, the rejection of claim 5 should be withdrawn.

Claims 6-12 and 52 depend from claim 5, and are believed to be allowable for at least the same reasons.

CONCLUSION

In view of the foregoing amendments and remarks, this application should now be in condition for allowance. A notice to this effect is respectfully requested. If the Examiner believes, after this amendment, that the application is not in condition for allowance, the Examiner is requested to call the Applicants' attorney at the telephone number listed below.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicants hereby request any necessary extension of time. If there is a fee occasioned by this response, including an extension fee that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Respectfully submitted,

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